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DESIGN AND ANALYSIS OF 1-BIT FULL SUBTRACTOR FOR ARITHMETIC APPLICATIONS IN EMBEDDED SYSTEM

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ABSTRACT

In modern VLSI design, static or leakage-power consumption is a crucial metric due to the miniaturization of components. In this project work, a 1-bit complete circuit using only 10 transistors is suggested and compared to alternatives using both 20 and 14 transistors.

All circuit simulations were carried out using the CAD programme Micro wind 3.1.

Subtractor layout for feature size 90nm technology has been used to derive values for a variety of parameters.

When compared to its competitors, the energy efficient of the suggested 10-transistor complete subtractor stands out.

I. INTRODUCTION

1.1 INTRODUCTION TO VLSI:

Very large scale integration is frequently abbreviated to VLSI. With the advent of very large-scale integration (VLSI) technology, the electronic sector has experienced unprecedented expansion over the past two decades. In addition, the intelligence of these applications, or the processing power they demand, is the sole driving force behind the explosive growth of the sector. For video and cellular communication, low bit rate is now cutting edge since it gives customers a certain degree of processing power and portability.

In 1958, Jack Kilby of Texas Instruments created the first integrated circuit flip-flop out of just two transistors. More than two billion transistors are included in Intel's Itanium processor, and more than four billion transistors are present in the 16 GB of Flash memory. Over the next 50 years, the integrated circuit industry is expected to increase at a rate of 53% every year. There hasn't been any innovation that saw such rapid expansion for so long. Consistent reductions in transistor count and size, as well as advancements in processing technology, enable this phenomenal expansion. The 3p's (performance, power, and cost) are a balancing act in most other areas of engineering as well. However, when transistor size drops, power consumption reduces, space occupied reduces, performance increases, and the cost to manufacture decreases.

Electronic circuits throughout the first half of the 20th century are bulky, power-intensive, cost-prohibitive, and unreliable since they rely on vacuum tubes. In 1947, at Bell Labs, John Bardeen and Walter Brattain created the first working point contact transistor. Bell Labs introduced the technology to the public, but it was a military secret at the time. Transistor. Because it acts as an amplifier and transfers resistance between terminals, scientists dubbed it the transistor.

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An electrical signal can be amplified and transferred between the input and output terminals of a transistor, a semiconductor device. There is no vacuum, no glass tube, and no filament. All of its elements are chilly and solid.

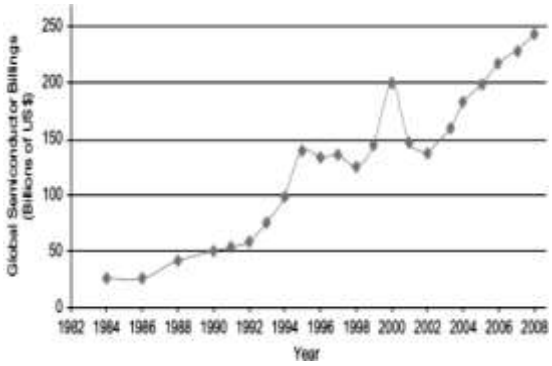

Figure 1: Quantity of semiconductors sold around the world

A transistor consists of a control terminal and two additional terminals that connect or detach based on the voltage or current applied to the control terminals, and hence can be thought of as electrically controlled switches. BJT was created by Bell Labs not long after the point contact transistor was first introduced. There is a considerable improvement in reliability, noise immunity, power efficiency, and speed in bipolar devices. For early IC designs, BJTs were the norm. Bipolar transistors can only switch bigger currents between the emitter and collector terminals when modest currents are supplied to the base terminal. The greatest number of transistors that can be integrated on a single die is capped due to the transistors' quiescent power dissipation caused by base currents, drawn even when the circuit is not switching. Production of MOS Transistors started in the 1960s. When not conducting, the MOS transistor provides almost no current. They are available in NMOS and PMOS varieties. The German physicist Julius Lilien field came up with the concept of field effect transistors in 1925, and Oskar Heil presented a structure similar to the MOSFET in 1935, but early attempts to construct operational devices were thwarted by issues with the materials used.

In 1965, Gordon Moore noticed that the number of transistors that could be made most cheaply on a chip followed a straight line on a semi-logarithmic scale. He discovered that the number of transistors in electronic devices doubles every half a year. Moore's Law is the name given to this observation, which has come to fulfil itself. Transistor count for Intel processors is depicted in Fig. 1.1.1. Increasing chip size and decreasing transistor size are both contributing factors to Moore's Law. Chips can be categorized by their level of integration into SSI, MSI, LSI, VLSI, or ULSI.

Figure 2: CPU transistors from Intel.

Less than ten gates and about six transistors per gate characterize small-scale integration (SSI) circuits like the inverter (IC 7404). The counter (IC74161) is an example of a medium-scale integration circuit. It

includes thousands of gates. Even a basic 8-bit processor uses up to 10,000 gates in a large-scale integration circuit. It quickly became evident that fresh names will be required every five years. If current terminology preferences persist, VLSI will be used to characterize the vast majority of ICs produced after the 1980s. Dennard's Scaling Law [Dennard74] is similar to Moore's law in that it states that as transistors get smaller, they get quicker, use less power, and are cheaper to produce. Time-to-execute-an-application benchmarks show that computer performance has improved even more than raw clock speed. Currently, the number of cores on a semiconductor determines performance rather than the clock speed. Compared to a single transistor, the power requirements of an integrated design are extremely high. This is because numerous transistors are involved in the design. Furthermore, as transistors have shrunk in size, they no longer switch off entirely. With millions or billions of transistors on a chip, even a small amount of current escaping through each transistor now results in enormous power consumption.

1.2 INTRODUCTION TO 90nm TECHNOLOGY

The first company to release an Industrial 65nm process was Toshiba in 2002, followed by Fujitsu, STM, NEC, and Intel in 2004. Following the release of their own techniques, IBM, Motorola, TI, TSMC, and Samsung.

Table I: What's special about 90nm technology

Feature	Foundry				
	Intel	ST Microelectronics	Fujitsu	Toshiba	NEC
V_{DD}(V)	1.1/1.2	0.9/1.1	1-1.2	0.85	0.9-1.2
Effective gate length (nm)	35	45	30/50	30	40
Oxide thickness (nm)	1.2	1.2	1.1-0.7	1.0	1.1- 1.35
# of metal layers	8		12	up to 13	
Interconnect layer permittivity K	2.9		2.25-2.9	2.7	2.5-2.9
Reference	[8]	[7]	[5]	[3]	[6]

The advantages of 90nm technology over 180nm are:

- Increases in velocity of 1.20 times
- There is a doubling in density.
- A halving of power output

Process variants in 90 nm technology:

Several variations on the 90nm technique are now in use. Maximum speed at the expense of a massive leakage current is represented by a value of 1. Due to its focus on high-speed devices like fast processors and digital signal processors, this technology is classified as "high speed" and is therefore absent from the Microwind 90nm rule file.

The second technological alternative, general purpose, is aimed at commodity items in which the speed factor is not crucial and features a leakage current that is an order of magnitude lower than that of the high speed variation while also reducing the gate switching delay by 50%.

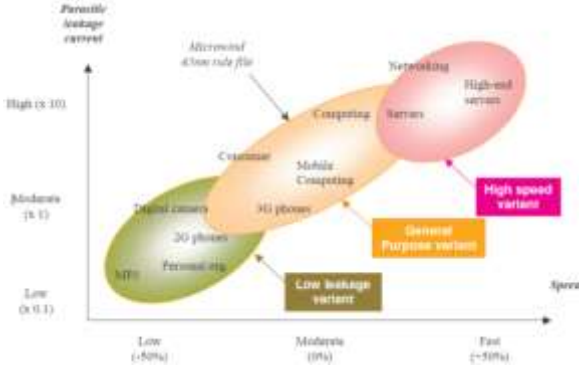

Figure 3: There are now three distinct 90nm process variations available.

The third type, low leakage, is used for integrated circuits (ICs) in which leakage must be kept to a minimum, such as in embedded devices, mobile phones, etc.

In 90nm technology, the operating voltage can range from 0.85 V to 1.2 V. In the instance of Microwind, the rule file has it set to 1V as a middle ground between the several possible processes.

1.3 LOW POWER VLSI:

There is no other source of energy on Earth but the sun and nuclear power. Over billions of years, the Earth has stored the energy of the sun in the form of plant growth, which has been converted to carbon and later to oil, gas, coal, or other carbon-based fuels, making it function like a massive battery. These days, we may also harness energy from the wind, tides, and precipitation (hydro) or the earth itself (geothermal) in addition to the sun (solar power). Changes occur in the form of energy. The importance of sunlight to plant development. To carbon, via plants. Coal to flame. Heat into usable energy. Powering batteries using electricity. Converting chemicals into energy (discharged batteries). Power to music (through an MP3) by electrical current. The last transformation releases a portion of the energy as sound waves into space. As the music is deciphered and performed, the rest is converted into heat. It has been dispersed throughout space (maybe warming our fingertips slightly on a cold night) and is now gone forever. Energy changes are so ubiquitous in our daily lives that we usually have no idea they are happening. Most of the time, they happen without anyone noticing.

Batteries eventually die and must be recharged or replaced. Designers of consumer electronics are always looking for ways to improve their products, whether it's through new features, smaller form factors, or longer battery life. The constant need to lessen reliance on fossil fuels and cut down on greenhouse gas emissions compels us to seek for low power solutions for all electronic difficulties in applications that are permanently plugged into an electrical outlet. About 150 watts is the upper limit for high-performance chips before liquid cooling or other expensive heat sinks are required. The electricity needs of American data centers and servers totaled 61 billion kWh in 2006 [EPA07]. This is equivalent to the production of 15 power plants, would cost around $4.5 billion, and would use 1.5% of the total energy utilized in the United States. Whereas the size of a chip used to be a limiting factor in its capabilities, today it is typically power consumption. High-performance design now automatically means energy-efficient design.

1.4 Power Optimization Methods

Below, we will go over how minimizing voltage, capacitance, and switching activity can help save power.

1.4.1 Voltage

Reducing voltage, which has a quadratic relationship to power, is the most efficient way to cut down on energy use. A reduction of the supply voltage by a factor of two results in a reduction of the power consumption by a factor of four without the need of any special circuits or technologies. This reduction in power consumption is not localized to any one chip's sub-circuit or block, but rather permeates the entire layout. These considerations explain why engineers so frequently opt for lower voltage at the expense of greater physical capacitance or higher circuit activity. Unfortunately, there is a trade-off in speed as we decrease the supply voltage, with delays becoming increasingly severe as VDD gets closer to the threshold voltage VT of the devices. Because of this, VDD is typically only effective between roughly 2-3 VT. The below equation shows that the strategy incurs a cost in the form of a reduction in switching speed.

$$T_d = \frac{C_{out}V_{dd}}{I} = \frac{C_{out}V_{dd}}{\eta\left(\frac{W}{L}\right)(V_{dd}-V_t)^2}$$

II. POWER ANALYSIS IN CMOS CIRCUITS

2.1. INTRODUCTION

Digital CMOS circuits' power dissipation can be modelled as:

$$P_{avg} = P_{dynamic} + P_{short\ circuit} + P_{leakage} + P_{static}$$

Where Pavg is the average power dissipation, P dynamic is the power dissipation caused by the switching of transistors, P short circuit is the power dissipation caused by a short circuit between the power supply and ground, P leakage is the power dissipation caused by leakage currents, and P static is the power dissipation caused by static electricity.

2.1.1 DYNAMIC POWER DISSIPATION

Charging and discharging capacitances in the circuit generate the dynamic power dissipation P dynamic. As illustrated in Figure 2.1, we will use a CMOS inverter supplying power to a load capacitor CL to demonstrate how dynamic power dissipation is calculated. The output capacitor is the sum of the parasitic capacitances of the Nmos and Pmos transistors (gate-to-bulk and source- and drain-diffusion to bulk), the inverter cell's internal and external wiring, and the circuits driven by the inverter.

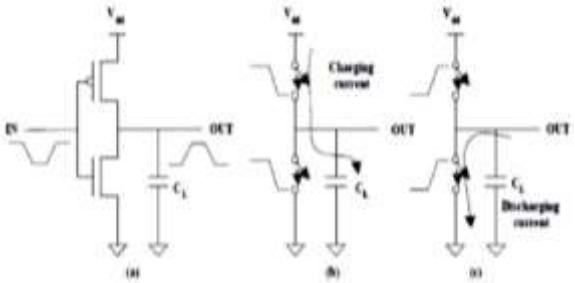

Figure 4: The three phases of a CMOS inverter's operation are as follows: (a) CMOS inverter, (b) charging, and (c) discharging.

Since the output capacitor can be connected directly to ground, a discharge current can flow through it. The load capacitor's 12 CL.V2dd of energy is wasted in the Nmos transistor and the connection. This means that across the range [0, T], the dynamic power dissipated by a CMOS inverter may be calculated as:

$$P_{dynamic} = C_L.V^2_{dd}.N_{0?\ 1}.1/T$$

2.1.2 POWER REDUCTION APPROACHES OF DYNAMIC DISSIPATION.

The average switching power dissipation P dynamic of CMOS logic gates is shown to be related to the load capacitance CL, the square of Vdd, the switching activity, and the clock frequency f, as shown by the derived equation.

Thus, the power reduction can be accomplished in a variety of ways, including (but not limited to) the following:

(i) decreasing the output capacitance CL (or the switching activity),

(ii) decreasing the power supply voltage Vdd (or the average number of transitions per clock cycle), and

(iii) decreasing the clock frequency.

Combining two or more of the aforementioned methods apparently allows for minimal power reduction. The effective capacitance, or switched capacitance, is the product of the output capacitance and the switching activity, and its decrease is a common low power method.

If a designer wants to cut down on power consumption, he or she should focus on two primary areas: lowering the voltage supply and increasing the effective capacitance. Since power savings are

proportional to the square of Vdd, one of the most aggressive methods involves lowering the voltage at which the supply operates. While this type of reduction is typically quite effective, it requires the designer to address a number of critical aspects to ensure the system's performance is not compromised. Delay propagation (or the rate at which a circuit moves) increases when the supply voltage is lowered. The transition of industry from a supply voltage value to a smaller one is quite costly and slow since the input and output signal levels should be compatible with the peripheral electronics. In contrast, new design methods are mostly responsible for lowering switching activity and/or capacitance for a given technology. As a result, instead of spending a tons of money on brand new equipment, a low-power version of an existing circuit can be built. Several circuit-level design strategies, such as optimized logic synthesis and balanced routes, must be implemented in order to reduce switching activity, and a thorough examination of signal transition probabilities is essential. By downsizing transistors and choosing the right logic family, for example, the output capacitance can be decreased. The Pentium-I consumed 15 watts of electricity at 5 volts and 66 megahertz (MHz), while the Pentium-II consumed 8 watts at 3.3 volts and 133 MHz, respectively.

2.1.3 SHORT-CIRCUIT POWER DISSIPATION

The energy lost in a short circuit During the switching phase, pshortcircuit occurs when current flows through the direct path between the power source and the ground. Think about the CMOS inverter from Figure1.4 again. Short-circuit current flows between the power supply and the ground during the extremely brief time interval in which both Nmos and Pmos transistors are ON when the input signal transitions from the logic value '1' to the logic value '0', or vice versa. A CMOS inverter's response to a short circuit is seen in Figure 1.2. Specifically, the Nmos transistor of the inverter circuit conducts if the input voltage rises beyond the threshold voltage, Vthn, and the Pmos transistor conducts until the input voltage reaches the value of (Vdd - |Vthp|). That's why there's a window of time when both transistors are active. As the output voltage drops, the Nmos transistor is discharging the capacitance CL. The Pmos transistor can conduct because the drain-to-source voltage drop is no longer zero. When the input voltage transition is complete, the Pmos is turned off, ending the short-circuit current. In the case of a symmetrical inverter with identical rise and fall periods, the output waveform begins to climb as both MOSFET transistors are ON due to the short-circuit current component originating from the falling edge of the input signal.

Total power consumption is calculated by averaging the short-circuit current component of the rising edge of the input signal with the equivalent current component of the falling edge.

III. LITERATURE REVIEW

With the proliferation of battery-powered mobile devices like smartphones, PDAs, and laptops, manufacturers are under pressure to create VLSI and ultra-LSI designs with better power delay characteristics. One of the most fundamental building elements of all these circuit applications is the full adder/subtractor, therefore studying it has been a primary focus of researchers for many years. To construct 1-bit complete adder cells, many different logic models were explored, each with their own benefits and drawbacks. Generally speaking, the reported designs can be broken down into two groups: 1) static styles, and 2) dynamic styles. In comparison to their dynamic counterparts, static logic designs are typically more secure, easier to implement, and less demanding of power, at the expense of a larger on-chip footprint.

A paper proposing a reversible logic gate was presented in 2012 by Parminder Kaur[et al. Many studies highlight reversible logic gates as the newest area of study. In this paper, the author pursues a fault-tolerant complete adder. The design may function independently as a full adding and subtracting unit. The

inputs and outputs both have the same parity, as this is a reversible adder cell that preserves parity. Any desired Boolean function can be synthesized with the help of the suggested parity-preserving reversible adder. It makes it easy to spot any problem with the circuit at the principal outputs if it only impacts a single signal. The suggested solution is more effective than existing alternatives while also requiring less hardware complexity because to its reduced gate count, garbage outputs, and constant inputs.

Prashanth[et al.] published the reversible logic gate in 2013. Low-cost CMOS design has recently benefited from the development of reversible logic gates. Quantum computing, nanotechnology, and optical commuting are just a few of the many uses for reversible logic gates. An effective fault-tolerant carry skip adder/subtractor is proposed here. This document also includes the designs for a complete adder/subtractor and a parallel adder/subtractor, which are prerequisites for creating a carry skip adder/subtractor. In terms of gate count, constant input, garbage output, and quantum cost, all of the designs in this study are effective. The proposed design is an all-in-one adder and subtractor that performs as either function depending on the control logic input. The design of a Carry skip adder/subtractor requires knowledge of both the Full adder/subtractor and the Parallel adder/subtractor.

A work on the Reversible Logic Gate was presented in 2014 by Dondapati Naresh[et al]. In the very-large-scale-integration (VLSI) realm, reversible logic gates are crucial. These days, it's used for a wide variety of tasks, including quantum computing, optical computing, cellular automata and digital signal processing on quantum dots, low-power CMOS architecture, and nanotechnology. In this study, we suggest a fault-tolerant carry skip adder/subtractor that employs reversible logic gates that preserve parity. The suggested architecture can function as either a carry skip adder or a carry skip subtracter, depending on the control logic input. When ctrl is set to zero, the design functions as a parallel adder, and when it's set to one, it functions as a parallel subtractor, according to the control logic input.

S. Mounika[et al.] published a study advocating for reversible logic as a promising new area for low-power computing in 2015. It will be useful in numerous fields, including computers (both quantum and classical), nanotechnology, optical computing, and others. A fault-tolerant carry-skip adder and subtractor is proposed here. This document also includes the designs for full and parallel adders and subtractors, which are prerequisites for creating a carry skip adder/subtractor. In terms of gate count, constant input, garbage output, and quantum cost, all of the designs in this study are effective.

Subramanian Saravanan[et al.] published an article in 2016 describing Optical information processing, low-power CMOS design, DNA computing, etc. are just a few of the many potential new areas where reversible logic is being put to use. Comparators are crucial in industrial automation as they separate bad patterns from good ones. These comparators have been developed in the past, albeit with a higher computational cost and number of reversible gates. Each of these comparators utilizes a form of "propagation" to examine the data. The comparators' performance will suffer as a result of this. To address this issue, the authors of this study present a (Thapliyal Ranganathan) TR gate-based efficient comparator that makes use of a complete subtraction and a half subtraction approach to boost computational speed. Quantum efficiency is enhanced by the comparator layout that makes use of the half subtraction technique. The entire subtraction method is used in the comparator design, which successfully decreases the number of reversible gates and eliminates garbage output.

IV. SUBTRACTOR CIRCUITS AND EXISTING SYSTEMS

4.1 SUBTRACTOR

One of the four elementary operations in binary, subtraction is the primary function of a subtractor, a digital circuit. Subtractors are used extensively in many computer and other device processors, and not

just for arithmetic computations. This includes areas where it is necessary to calculate addresses, table indexes, and similar operations. Moreover, it can be an Attenuator in various situations.

Most subtractors work with binary integers, but they can be built for other binary code representations like excess-3 or grey code or even binary-coded decimal. Two's complement or ones' complement is frequently used to indicate negative integers when subtracting two positive values. Modifying an adder into an adder-subtractor is often seen as somewhat important due to the simplicity with which computations can be conducted. A more complicated subtractor is needed for other signed number representations.

Inputs to the circuit device can range from two to three, depending on the nature of the application or the desired outcome of the task at hand. If we have two inputs, we can use a Half-Subtractor, and if we have three, we can use a Full-Subtractor.

When performing subtraction between two bits, a complete subtractor takes into account a third bit, called a borrow bit, from another circuit. Therefore, it accepts input from three separate bits. Two bits, difference and borrow, are produced as a result. Everywhere we go, we encounter various forms of digital media, including smartphones, computers, televisions, video game consoles, and so on. We must carry out the arithmetic operations in the devices' CPUs. One of the most fundamental arithmetic operations is subtraction. One bit, two bits, etc., can be subtracted using a subtractor. There must be at least three inputs for a full subtractor of one bit. Traditional CMOS technology allows for the building of a complete subtractor.

A full subtractor is a combinational circuit that uses the minuend, subtrahend, and borrow-in bits to execute subtraction. Full subtraction produces Difference and Borrow as output. In this post, we break down the XOR gate as a whole subtractor. Used in addition to the NOT gate, AND gate, and XOR gate. The gate level diagram of a full subtractor is displayed in Fig. 2.5. In this case, a full subtractor is constructed by joining two half subtractors.

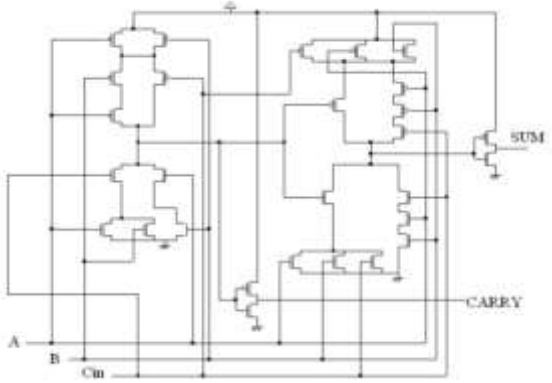

Fig 5. In CMOS, a complete subtractor with 20 transistors

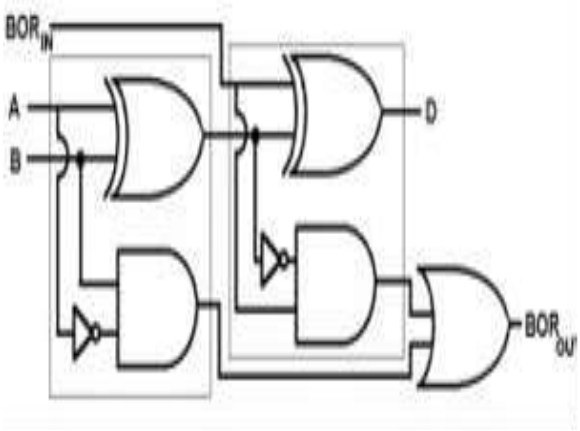

Fig 6. All-gate subtraction circuit

Input			Output	
A	**B**	**BORin**	**D**	**BORout**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 4.1 below displays the truth table for a full 1-bit subtractor..

If we examine how the Full-Subtractor operates, we see that it is possible to subtract the two given binary values by first adding the complement of the subtrahend to the minuhend. This technique can also be used to transform the subtraction operation into an addition operation that can be implemented in machines using complete adders. Now, in a direct subtraction method using logic circuits, each subtrahend bit of the number is subtracted from its corresponding significant minuhend bit to generate a separate bit. A 1 is "borrowed" from the next most significant position if the minuhend bit is less than the subtrahend bit.

Simply put, the Full-Subtractor performs a subtraction operation between two bits (a minuend and a subtrahend) while also accounting for whether or not a '1' has been borrowed by the preceding adjacent lower minuend bit. Therefore, a Full-Subtractor takes in three bits—the two bits to be subtracted and a borrow bit named Bin—at its input. Difference (D) and Borrow (Bo) are the two possible results. The Borrow output bit indicates whether or not the lowest minuend bit requires a '1' to be "borrowed" from the next available highest minuend bit.

The equations provide the Boolean expression for the two output variables.

$$D = A'B'Bin + A'BBin' + AB'Bin' + ABBin$$

$$Bo = A'B'Bin + A'BBin' + A'BBin + ABBin$$

4.2. ONE BIT FULL SUBTRACTOR BY USING 20 TRANSISTORS

Figure 4.1 depicts the circuit layout for a 20-transistor 1-bit full subtractor. When compared to standard full subtractor architectures, full subtractor designs use less transistors. To create a full subtractor, 6 transistors are used for the difference equation, 10 for the borrow equation, and the final 4 for the inverting operation.

In this study, we seek to use the extensive literature on adder design to create a one-bit complete subtractor with a minimal number of transistors. Twenty transistors make up the circuit; one 6-transistor EX-OR module, two CMOS inverters (one at the difference output and another at the borrow output), and a 10-transistor section that generates the borrow in accordance with the input bit variation make up the rest. Ten transistors, five PMOS and five NMOS, make up the borrow section, which is analogous to the carry section in a standard 1-bit full adder. Comparing the truth tables of a one-bit adder and a one-bit subtractor reveals that their respective outputs sum and difference are identical, while the adder's output carry differs in four of the eight possible results.

Three PMOS transistors (M1, M3, and M5) and three NMOS transistors (M2, M4, and M6) make up the 6T XOR gate, four transistors (M7, M8, M19, and M20) function as two inverters, and transistors (M9, M10, M13, M14, and M15) from the PMOS side and transistors (M11, 12, 16, 17, and 18) from the NMOS side manage the borrow function. When A=1, B=1, and C=1 are used as inputs, the difference output should be 1 and the borrow output should be 1.

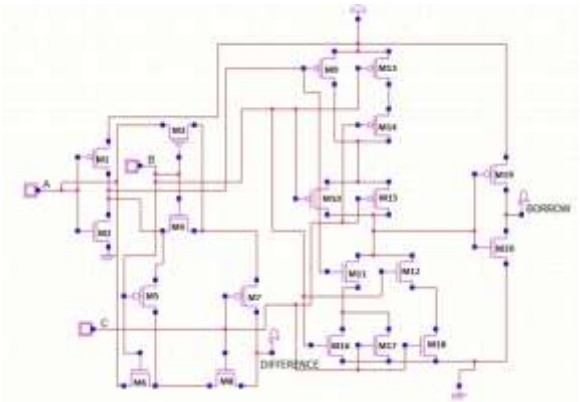

Fig.7 A full-bit, 1-transistor subtractor

4.3. ONE BIT FULL SUBTRACTOR USING 14 TRANSISTORS

Figure 4.3 depicts the 14 transistors needed to create the XOR-XNOR modules and 2x1 multiplexer that make up the one bit full subtractor circuit. Two intermediate signals are generated by the XNOR - XOR modules and sent to the 21 multiplexer. The output of the aforementioned logic gates serves as one input to a 21 multiplexer, while the output of the third input serves as the multiplexer's selection line. A 6T

XOR-XNOR cell and a multiplexer provide the difference output, whereas a 6T XOR gate produces the borrow output. Transistors M1, M2, M3, and M4 all use the 4T XOR module. Combining the XOR module's four transistors with the XNOR module's two, we get a 6T XOR-XNOR module. To create a 2x1 multiplexer, transistors M9 and M10 are used here. Bit C is the multiplexer's choose or control input. However, besides OR and NOR, XOR and XNOR are also used to provide inputs to this multiplexer. The difference output of the subtractor is the XNOR output if C=1, and the XOR output if C=0. The input combination and the other module, a 6T XOR-XNOR cell and a multiplexer, generate the borrow output. Modules M7, M8, M11, M12, M13, and M14 are all 6T XOR modules. The XOR CELL based feedback inverter is the main component of this setup.

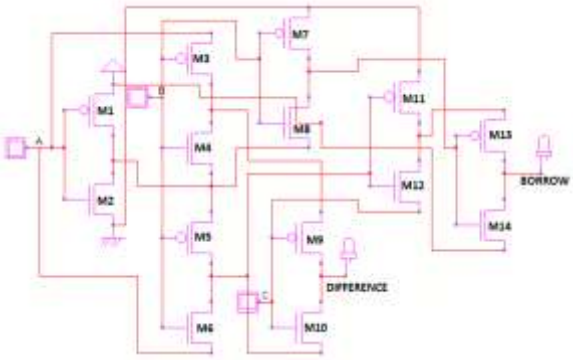

Fig.8. Fourteen-transistor full-bit subtractor for one bit.

V. PROPOSED METHODS

These days, one of the most difficult challenges in the design of digital integrated circuits is overcoming the power consumption and sub threshold leakages. A microprocessor chip is the foundation for expanding both the functionality and the density of transistors. The scaling function contributes to the integrated circuit design's improved performance as well as its increased speed of operation. Leakage current and power are two issues that frequently arise in the design of digital circuits in the modern day. Improving the digital system's reliability can be performed by reducing the circuit's physical size, weight, and cost. This can be accomplished by cutting down on the number of transistors used in the design of the circuit.

ONE BIT SUBTRACTOR USING 10 TRANSISTORS

Figure 4.2 presents the logic circuit of a one-bit complete subtractor design that makes use of two XOR gates and one multiplexer. This design has three inputs, such as A, B, and C, and two outputs, which are labelled Difference and Borrow respectively. The implementation of the transistor level circuit consists of four XOR gates built out of transistors, as well as a two-transistor 2x1 multiplexer. In addition to this, the differential outputs are derived from second XOR gates and are borrowed from the multiplexer.

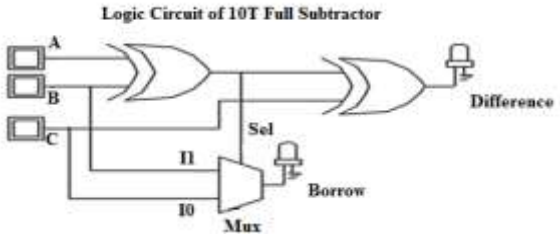

Fig 9. A full subtractor logic cell with only one bit proposed.

The multiplexer takes the logic value from the output of the first XOR gate, which is treated as a selection line. The multiplexer takes inputs from both the B and the C.

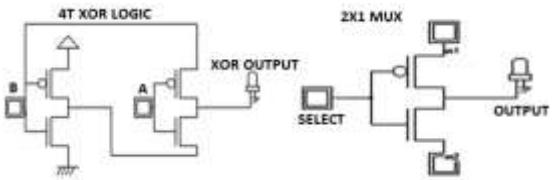

Fig. a Fig. b

Fig.10 a) (b) The total number of XOR gates and multiplexers in the circuit.

The XOR gate and multiplexer transistor-based circuits are depicted in (a) and (b) of Figure 6.2. The circuit diagram for a 10-transistor-strong complete one-bit subtractor is depicted in Figure For the first EX-OR gate, we use the first four transistors (M1, M2, M3, and M4), and for the second, we use the fifth through tenth. Multiplexer components M7 and M8 are a pair of transistors. With some tweaks to the connections and the choice of input combination to the multiplexer, the suggested design was based on a 10T one-bit full adder. Here, the choose line leading out of the first XOR cell is the input to the second XOR cell and a multiplexer. The difference output is the complement of input bit C if the first XOR output is at logic 0; otherwise, the difference output is the same as input bit C only. Borrow output is input bit C only if the first EX-OR output is a logical 0. Similarly, if the first output of an EX-OR gate is logic 1, then only input bit B will be borrowed at the output. Figure 5.8 shows the timing waveforms for all the possible input bit combinations, illustrating the full operation of the device.

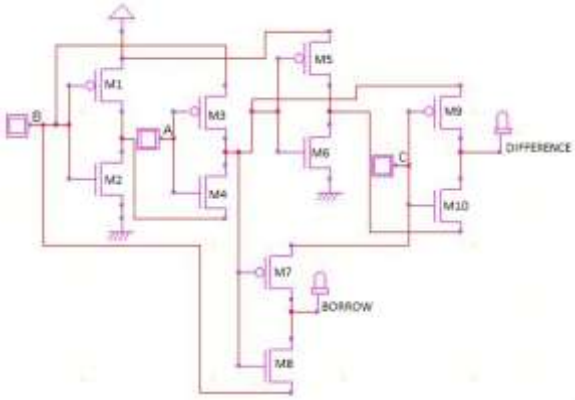

Fig.11 A 10-transistor, 1-bit subtraction circuit.

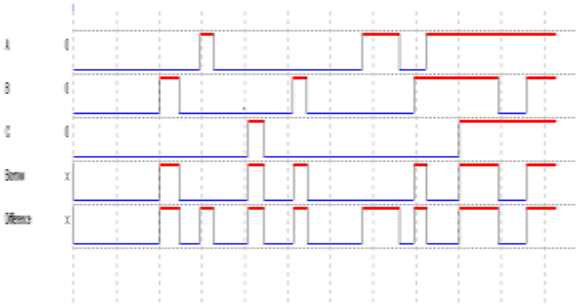

Fig.12 The timing waveform of a 10-transistor, 1-bit complete subtractor.

VI. RESULTS AND DISCUSSIONS

All of the simulation in this work was performed at 90nm technology using the CAD tool Microwind 3.1, and several different low-transistor-count complete subtractor circuits were analyzed. Area, Power, and Delay were measured and compared to a standard complete subtractor with one bit of precision using the simulation results.

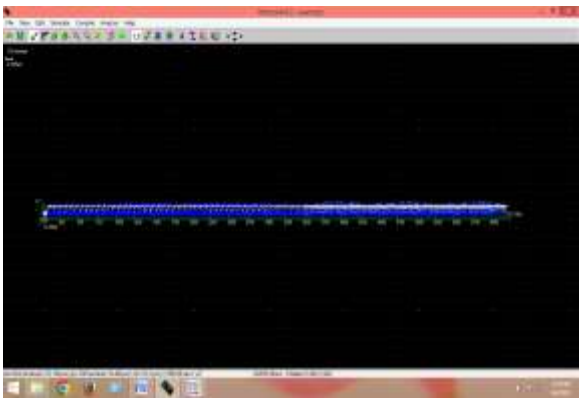

Fig.13. Microwind circuit area for 20 transistors.

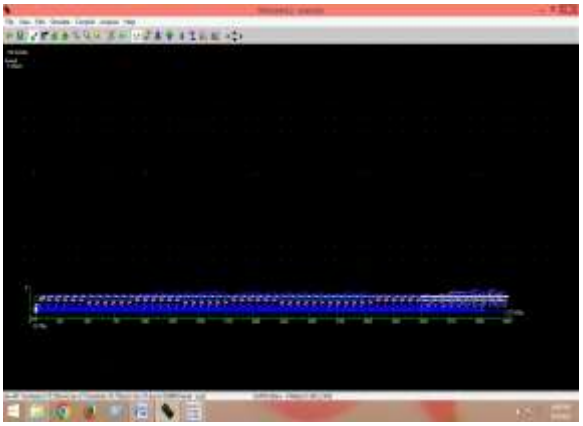

Fig.14. Circuit layout using microwind for 14 transistors

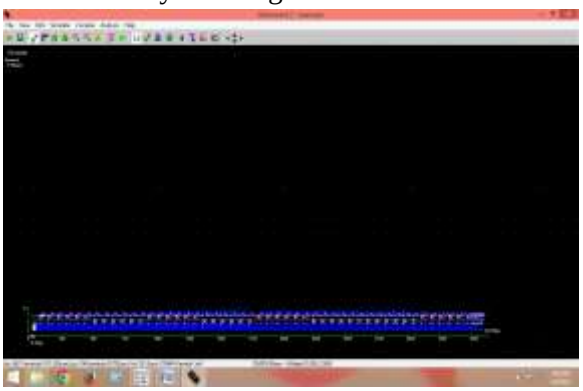

Fig.15. Circuit layout using microwind for 10 transistors

Fig.16. Timing and power consumption for a 20-transistor microwind circuit

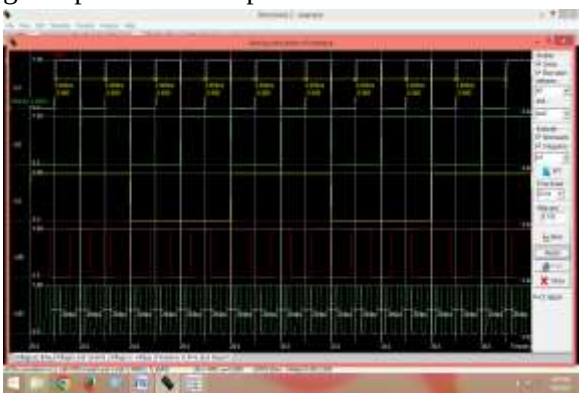

Fig.17. Timing and power consumption for a 14-transistor microwind circuit.

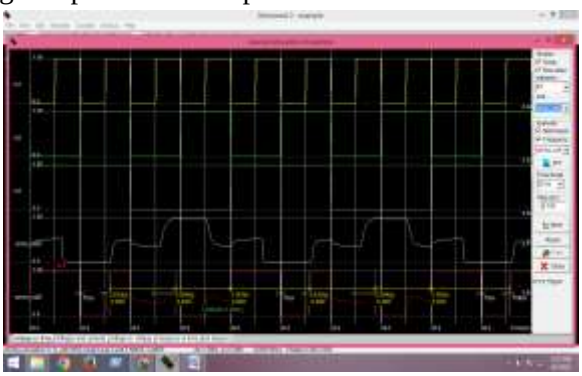

Fig.18. Power and delay in a microwind circuit with 10 transistors

DESIGN	DELAY(ns)	AREA(lamda)	POWER(micro W)
10 T	0.011	704414	15.176
14 T	0.200	926865	73.180
20 T	0.400	1298336	473.02

Table 7.1. The outcomes of various one-bit full subtraction circuit simulations. Table 7.1 compares the energy and EDP efficiency of one bit complete subtractors of 10T, 14T, and 20T and finds that the 10T version is the most effective.

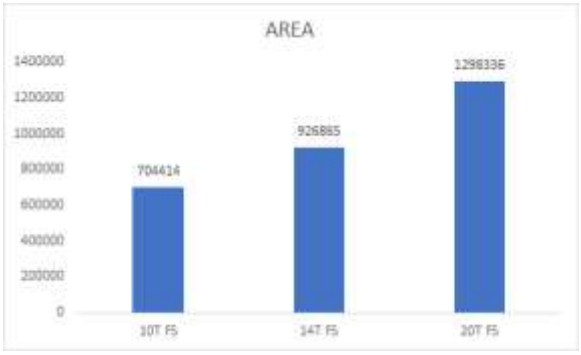

Fig 19: Comparative study of the footprints of many full-bit, one-bit subtractor circuits

Fig 20: Delay performance investigation of various complete subtractor circuits with 1 bit of precision

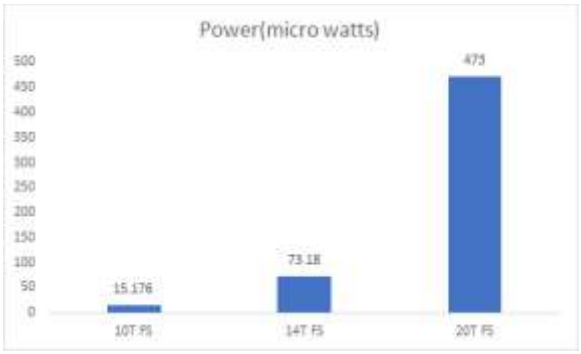

Fig 21. Comparison of power consumption over a range of 1-bit complete subtractor circuits

In figures 7.7, 7.8, and 7.9, we saw the results of our examination of the area, latency, and power consumption of several different kinds of one-bit complete subtractor circuits.

VII. CONCLUSION AND FUTURE SCOPE

CONCLUSION:

It can be seen from the outcomes that the 10T one bit complete subtractor uses less space than its competitors.

While the 10T one bit complete subtractor uses less power than its competitors, the delay it introduces is greater than that of the 14T and 20T versions.

As a result, the 10T one-bit complete subtractor saves on delay while using significantly less power and space.

FUTURE SCOPE :

In signal and image processing, the designed circuit can be utilized to construct a powerful multiplier.

Applications such as ADCs and DACs are making use of this technology.

The number of transistors in the Proposed 10-transistor design is currently the subject of investigation.

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